AMENDMENTS TO THE CLAIMS:

Please amend claims 1, 4 and 15 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) Apparatus for processing data, said apparatus comprising:

(i) a shifting circuit; ~~and~~

(ii) a bit portion selecting and combining circuit; and

(iii) an instruction decoder, responsive to an instruction to control said shifting circuit and said bit portion selecting and combining circuit, for performing ~~to perform~~ an operation upon a data word Rn and a data word Rm, wherein said operation yields a value given by:

~~(iv)~~ (a) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn;

~~(v)~~ (b) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction; and

~~(vi)~~ (c) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd.

2. (original) Apparatus as claimed in claim 1, wherein said first portion extends from a most significant bit end of said data word Rn.

3. (original) Apparatus as claimed in claim 1, wherein said first portion extends from a least significant bit end of said data word Rn.

4. (currently amended) Apparatus as claimed in claim 1, wherein said shift operand can specify ~~any~~a number of bit-positions representing an amount of arithmetic right shift to apply to said data word Rm.

5. (original) Apparatus as claimed in claim 1, wherein said first portion and said second portion abut within said output data word Rd.

6. (original) Apparatus as claimed in claim 5, wherein said output data word has a bit length of C and C = A + B.

7. (original) Apparatus as claimed in claim 6, wherein A = B.

8. (original) Apparatus as claimed in claim 1, wherein A = 16.

9. (original) Apparatus as claimed in claim 1, wherein B = 16.

10. (original) Apparatus as claimed in claim 1, wherein said instruction is a single-instruction-multiple-data instruction.

11. (original) Apparatus as claimed in claim 1, wherein said instruction combines a data value pack operation with a shift operation.

12. (original) Apparatus as claimed in claim 1, wherein said shifting circuit is upstream of said selecting and combining circuit in a data path of said apparatus.

13. (original) Apparatus as claimed in claim 12, wherein said selecting and combining circuit is disposed in parallel to an arithmetic circuit within said data path.

14. (original) A method of data processing, said method comprising the steps of decoding and executing an instruction that yields a value given by:

(i) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn;

(ii) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction; and

(iii) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd.

15. (currently amended) A computer program ~~product comprising~~provided on a computer-readable medium, said a computer program for controlling a computer to perform the steps of decoding and executing an instruction that yields a value given by~~a method as claimed in claim 14~~:

(i) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn;

(ii) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction; and

(iii) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd.